CLAIMS:

Claim 1. A phase detector for a phase locked loop to derive a control voltage for a voltage controlled oscillator VCO, comprising:

a charge pump, having complementary PMOS and NMOS switches, to charge a storage capacitor for deriving a control voltage for a VCO when said PMOS is on, and to discharge said capacitor when said NMOS is on;

a phase comparator for selectively generating a sourcing signal to turn on said PMOS and a sinking signal to turn on said NMOS;

a reset signal for inactivating said phase comparator when both sourcing signal and sinking signal are high, wherein said reset signal is derived from the gates of said PMOS and said NMOS switches through an AND gate.

Claim 2. The phase detector described in claim 1, wherein said sourcing signal is fed to the gate of said PMOS through a first inverter, and the gate of said PMOS is fed to said AND gate through a second inverter.

Claim 3. The phase detector as described in claim 1, further comprising a third inverter and a fourth inverter in series between said sinking signal and said AND gate to introduce a delay to the NMOS for compensating the intrinsic delay of said PMOS.

Claim 4. The phase detector as described in claim 1, wherein said PMOS and said NMOS switches are a PMOS cascode amplifier and an NMOS cascode amplifier.

Claim 5. The phase detector as described in claim 4, further comprising a fifth inverter and a sixth inverter in series between said sinking command and the input gate of said NMOS cascode amplifier.

Claim 6. The phase detector as described in claim 4, further comprising a first capacitor connected between a positive power supply and the gate of the output PMOS of said PMOS cascode amplifier, a second capacitor connected between a negative power supply and the gate of the output NMOS of said NMOS cascode amplifier.

Claim 7. The phase detector as described in claim 1, further comprising a seventh inverter and an eighth inverter in series between said AND gate and said phase comparator.

Claim 8. The phase detector as described in claim 4, further comprising a ninth converter and a tenth converter in series with a negative reference voltage of the PMOS cascode amplifier, and an

eleventh converter and twelfth converter in series with the positive reference voltage of the NMOS cascode amplifier.

Claim 9. The phase detector as described in claim 4, wherein the input switches of the PMOS cascode amplifier and the NMOS cascode amplifier are current switches.